Chirag Kantharia

Summary

- Experienced system software developer with over 17 years of experience, passionate about building products that sustain test of time, with proclivity for minimalism, beautiful code and elegant architecture. Identifying bottlenecks, building productivity tools, automating work flows are my areas of interest.

Skills

- Platform software, Control plane software, DPDK, L2/L3 Networking, Routing
- Virtualization (QEMU/libvirt), Messaging frameworks, Configuration management, Build systems
- Linux/FreeBSD/JUNOS Kernel, Device drivers, System software, Board bringups
- C, Python, nodejs, make, GDB, Git, SVN, CVS

Experience

Jan 2017 - Present **Software Engineer/Co-Founder**, *Korero Systems*, Bangalore, India.

- I designed the core product offering which is responsible for responding to customer queries on the phone aka Virtual Call Center. I developed a NodeJS based service backend which runs on AWS cloud and retrieves information from a Service.Now instance and attends to customer queries using Amazon Lex framework.

Jan 2015 - Dec 2016 **Software Engineer**, *Versa Networks Inc*, Bangalore, India.

- I co-developed and maintained high availability framework for Versa routing platform. The framework consisted of publisher-subscriber model based network state notification to achieve control plane and data plane redundancy on Versa routing platform which formed the basis for intra-chassis and inter-chassis redundancy feature on the platform. I also co-developed an HA notification library used by control plane daemons to switch to active mode or to standby mode upon mastership switchover. Additionally, I worked on VRRP based solution for traffic failover to standby node upon active node failure.
- I maintained the filter manager daemon which kept track of filters/ACLs created by various daemons and programmed those in the Intel DPDK based dataplane on Versa routing platform.

Nov 2004 - Dec 2014 **Staff Engineer**, *Juniper Networks Inc*, Bangalore, India.

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- I developed publisher-subscriber model based server backend for an SDK for programmable networks. The backend enabled Juniper routers to push network events to control plane software running on an external box which could then take action on the event.
- I co-delivered hardened, high-performance service provider appliance, CSE2000, that acted as an external service card on PTX5000, which delivered wide range of controller, scaling and network function virtualization (NFV) applications. My responsibility was mainly the control plane software including chassis management which comprised of reading sensor data off I2C devices, managing alarm conditions, handling IPMI events, and pushing interface events to the main control board running JUNOS, thereby, enabling the appliance to appear as a pluggable in-field replaceable unit (FRU) to the the management software running on main control board. This also involved writing protocol handler for TNP, proprietary IP level protocol used on Juniper routers between various components, to Linux.
- I developed control plane software for T4000 line card, including board initialization, communciation with the control board running JUNOS, and remote upgrade procedure for the FPGA on the line card.
- I co-developed infrastructure for in-service software upgrade for Juniper T-series, M-series and TX-series routers. My responsibility comprised of the in-service upgrade control flow, and replication of kernel state across heterogenous kernel versions. The feature enables Juniper routers to carry out software upgrade in production environment with minimal traffic loss.
- I co-developed and maintained GRES (Graceful RE Switchover) infrastructure for high availability and redundancy for control plane objects, which comprised of replicating kernel state onto the standby node on Juniper routers with dual routing engines.
- I developed tools for monitoring scaling numbers for Juniper routers across releases. This helps the competitive edge team to ensure that Juniper routers scaled to the published numbers.
- I created a HAL abstraction layer making it easier to port JUNOS to new platforms. This enabled the porting of JUNOS effort equivalent of writing a device driver for the new platform. The modularization was flexible to allow addition of new platform specific routines if required. I, also, developed diagnostic software to validate new hardware including NICs and ethernet switches on the multiple Juniper platforms.
- Feature enhancement and sustenance of JUNOS kernel.

Jun 2003 - Oct 2004 **Senior Software Engineer**, *Hewlett-Packard*, Bangalore, India.

- I developed parallel boot mechanism for OpenSSI, Linux cluster project sponsored by HP, which helped faster bootup of the significantly large Linux cluster. I was also official release engineer for the project for several releases. I also helped beta customers to scale their applications on the cluster. I also helped port Linux Test Project to OpenSSI to help weed out bugs related to system call behaviour on the cluster infrastructure.

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- I maintained CPQARRAY, CPQFC device drivers in the mainline Linux kernel, and support for the drivers in HP volume manager utility. I created the distribution packages for various mainstream Linux distributions including RedHat and SUSE.

Mar 2002 - Apr 2003 **Software Engineer**, *Timesys Inc*, Bangalore, India.

- I ported Timesys Linux to various PowerPC and StrongARM based single board computers from Embedded Planet and Applied Data Systems, which comprised of getting the Timesys Linux to boot up on the board and getting the serial console and ethernet working. I also ported framebuffer device driver, microwindows, picogui on few single board computers with LCD display.

Dec 1999 - Feb 2002 **Software Engineer**, *Epigon Audiocare*, Bangalore, India.

- I developed a clean-room implementation of Java Virtual Machine adhering to J2ME/MIDP specifications intended to run on a Linux 2.2 based embedded system. The target system was a Netsilicon manufactured Net+Lx single board computer.
- I developed Linux 2.4 device driver for in-house developed PCI card for C-sound music synthesis. The device processed the C-sound input and generated MIDI files which could be downloaded by the user upon being notified by the driver.

Education

1995–1999 **B.Tech**, *Computer Science and Engineering*, IIT Bombay, Mumbai.

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